REMARKS

Claims 19, and 20 are presented for examination. Claim 22 has been cancelled.

Claims 19, 20 and 22 have been rejected under 35 U.S.C. 112, first paragraph, as being based on non-enabling disclosure. Further, claims 19, 20 and 22 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner takes the position that the recitation of circuitry corresponding to tail current source N22 of FIG. 4 or 6 is critical or essential.

To overcome this rejection, the Examiner suggests that claim 19 should recite a differential pair including the claimed first and second insulating gate transistors.

Claim 19 has been amended in accordance with the Examiner's suggestion to recite a differential stage including a first insulated gate transistor and a second insulated gate transistor.

However, the Applicant respectfully disagrees with the Examiner's assertion that the circuit of the present invention would not operate as a differential amplifier if N22 is missing. As shown, for example, in the US patent 5,550,493 to Miyanishi cited by the Examiner in the present application, an amplifier may operate as a differential amplifier even if a current source transistor is not connected to the differential transistors. Therefore, the applicant believes that the current source transistor is not critical to the operation of the present invention.

Claims 19, 20 and 22 have been rejected under 35 U.S.C. 102(b) as being anticipated by Bion et al.

To more clearly define the claimed invention, claim 19 has been further amended to recite the subject matter of claim 22 dependent from claim 19.

Claim 19, as amended, recites level detection circuitry for detecting a difference between a first voltage and a second voltage. The circuitry comprises a differential stage including a first

insulated gate transistor and a second insulated gate transistor. The first insulated gate transistor receives a power supply voltage as the first voltage at a gate thereof and has a first conduction node, and a second conduction node for outputting a difference signal. The second insulated gate transistor receives a reference voltage as the second voltage at a gate thereof and having a first conduction node connected to the first conduction node of the first insulated gate transistor. The second insulated gate transistor has a current supply ability different from a current supply ability of the first insulated gate transistor under a condition of the same gate voltage. The difference signal corresponds to a difference between the first and second voltages. The reference voltage determines a voltage level of an internal voltage generated from the power supply voltage.

Also, the level detection circuitry comprises:

-operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, the operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

-a buffer circuit for buffering the difference signal for generating a binary level detection signal indicating whether the first voltage is higher than the second voltage.

As demonstrated below, Bion does not disclose the claimed arrangement.

Considering the reference, Bion discloses a differential amplifier used as a comparator for reading data in a ROM (Fig. 12). Transistors 41 and 42 of Bion constitute a current mirror, transistors 39 and 40 constitute a differential pair, and transistor 43 is a current source. Buffer circuit 44 is a Schmidt trigger circuit to adjust the criterion level of H and L level of the output signal of the differential amplifier.

Bion provides an offset for setting the output signal to L level rather than to an intermediate level when the input signals to the differential pair are at the same voltage level. In order to provide the offset, the channel width of transistor 39 is set to be wider than that of transistor 40, and the size of transistor 42 is set to be greater than that of transistor 40.

In Bion, comparator 37 receives the power supply voltage through transistor 38 at the non-inverting input node, in order to compensate for the voltage drop via the precharging transistor 36 at the data read out node or the inverting input node. Bion detects whether the precharge voltage at the input node changes according to read out memory cell data, with the power supply voltage used as the reference voltage for the comparison.

By contrast, in the claimed invention, the power supply voltage is compared with the reference voltage to detect the voltage level of the power supply voltage itself. As a result, the internal voltage can be prevented from dropping excessively even at a lower limit operating region. Claim 19 specifically recites that the reference voltage determines the voltage level of the internal voltage generated from the power supply voltage.

Bion does not consider stabilization of the internal voltage. The reference only considers the access time in a data reading operation using an unbalanced differential buffer.

Hence, Bion does not teach or suggest the claimed arrangement.

In view of the foregoing, and in summary, claims 19 and 20 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

Entry of the amendment to claim 19 under 37 CFR §1.116 is respectfully requested because the amendment raises no new issues. In particular, the amendment to claim 19 complies with

requirements of form expressly set forth in a previous Office Action, and incorporates the limitation of cancelled claim 22 dependent from claim 19.

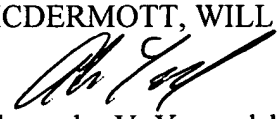
Attached hereto is a marked-up version of the changes made to the claims by the current amendment.

If there are any outstanding issues which might be resolved by an interview, Examiner is requested to call Applicant's representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 19 has been amended as follows:

19. (Twice Amended) Level detection circuitry for detecting a difference between a first voltage and a second voltage, comprising:

a differential stage including a first insulated gate transistor and a second insulated gate transistor,

[a] said first insulated gate transistor receiving a power supply voltage as the first voltage at a gate thereof and having a first conduction node, and a second conduction node for outputting a difference signal[;], and

[a] said second insulated gate transistor receiving a reference voltage as the second voltage at a gate thereof and having a first conduction node connected to said first conduction node of said first insulated gate transistor, said second insulated gate transistor having a current supply ability different from a current supply ability of said first insulated gate transistor under a condition of the same gate voltage, and said difference signal corresponding to a difference between the first and second voltages, said reference voltage determining a voltage level of an internal voltage generated from said power supply voltage;

operation current supply circuitry for supplying an operation current to the first and second insulated gate transistors, said operation current supply circuitry comprising a current mirror coupled to the first and second insulated gate transistors for supplying current to the first and second insulated gate transistors; and

a buffer circuit for buffering said difference signal for generating a binary level detection signal indicating whether said first voltage is higher than said second voltage.